CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA , 22313-1450 on 15 March 2006

Jeannie Camara

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Jeannie Camara

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PATENT APPLICATION
Attorney Docket No. 2442/127

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE PATENT APPLICATION OF	)
	) Examiner: Qureshi, Afsar M.
Robert A. Dickson et al.	)
	) Group Art Unit: 2667
Serial No. 09/995,356	)
	)
Filing Date: 27 November 2001	)
	)
Title: METHOD AND SYSTEM FOR BUFFERING A DATA PACKET FOR TRANSMISSION TO A NETWORK	)

O.K. to enter AP 4/11/06

AMENDMENT TRANSMITTAL LETTER

Mail Stop: AF
Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In connection with the above-referenced U. S. patent application, transmitted herewith are the following papers:

[x] Response under 37 C.F.R. § 1.111 to official action mailed **30 January 2006.**

[ ] A petition for extension of time is also enclosed with a fee of $55.00 for a one-month extension for a small entity.

[ ] Terminal disclaimer under 37 C.F. R. § 1.321(c), including

[ ] check for $110.00 fee under 37 C.F.R. § 1.20(d), and

[ ] 2 certificates under 37 C.F.R. § 3.73(b).

[ ] Information disclosure statement, form 1449 and ___ references.

[x] No additional claims fees are required.

[ ] An additional fee is required, and is calculated as shown below:

AMENDED CLAIMS					
	NO. OF CLAIMS	HIGHEST NO. OF CLAIMS PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	ADDT'L FEE
Total Claims		MINUS = 20	0	x $18 =	
Independent Claims		MINUS = 3	0	x $78 =	
If Amendment adds multiple dependent claims, add $260.00					
Total Amendment Fee					
If small entity status is claimed, subtract 50% of Total Amendment Fee					
TOTAL ADDITIONAL FEE DUE FOR THIS AMENDMENT					$0.00

[ ] A check in the amount of $___ is enclosed.
[ ] Charge $___ to Deposit Account No. ____ (Docket No. ___).
[x] Please deduct any underpayments, credit any overpayments, and charge all required extension of time fees to Deposit Account Number 50-1003. (Docket No. 2442/127).

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Respectfully submitted,

By 
Edward J. Grundler
Registration No. 47,615

Date: 15 March 2006

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Application Number	: 09/995,356	Confirmation Number: 2995
Applicant	: Robert A. Dickson et al.	
Filed	: 27 November 2001	
TC/A.U.	: 2667	
Examiner	: Qureshi, Afsar M.	
Docket Number	: 2442/127	
Customer No.	: 22,835	

M/S: Box AF
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir

In response to the office action of **30 January 2006**, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A packet buffer control system comprising:

a memory storing bytes of data in lines;

a packet buffer, the packet buffer divided into a first section and a second section, each section for storing bytes of data in lines; and

a packet buffer controller that receives a line of data from said memory along with a tag indicating a shift value, wherein the packet buffer controller is configured to shift ~~and shifting~~ said received line of data in accordance with the shift value for storage in said first section and in said second section and to store the resulting shifted line of data simultaneously ~~wherein storage~~ in said first section and in said second section ~~occur simultaneously~~.

2. (Original) The packet buffer control system of claim 1 wherein said packet buffer controller comprises a wrap-around shift register in which said received line of data is shifted for storage.

3. (Currently amended) The packet buffer control system of claim 1 further comprising ~~means~~ a mechanism for masking a line in said packet buffer.

4. (Currently amended) The packet buffer control system of claim 1 wherein ~~storage of a~~ the packet buffer controller is configured to store the shifted line of data in the first section and in the second section ~~is accomplished~~ in a

single clock cycle.

5. (Original) The packet buffer control system of claim 1 wherein the packet buffer controller further includes logic that reads a first output data line from the first section and then reads a second output data line from the second section for transmission to a network.

6. (Previously presented) A method of communicating alignment information comprising:

preparing read requests for lines of data to fill a packet payload;

obtaining a shift value corresponding to any misalignment between the lines of data and the packet payload;

sending a read request including a tag with the shift value, said tag being for inclusion in a response to the read request;

receiving at a packet buffer controller the response having a line of data and the tag; and

shifting the line of data in accordance with the shift value in the tag and writing the shifted line of data into a first section and a second section of the packet buffer, wherein writing the shifted line of data into said first section and said second section occur simultaneously.

7. (Original) The method of claim 6 wherein writing the shifted line of data is accomplished in a single clock cycle.

8. (Original) The method of claim 6 wherein said act of writing writes bytes of the shifted line of data that are in unmasked positions of the packet buffer into the packet buffer while bytes of the shifted line of data in masked positions of the packet buffer do not make changes to the masked positions of the packet

buffer.

9. (Original) The method of claim 6 further including:

reading a first output data line from said first section and then reading a second output data line from said second section for transmission to a network.